

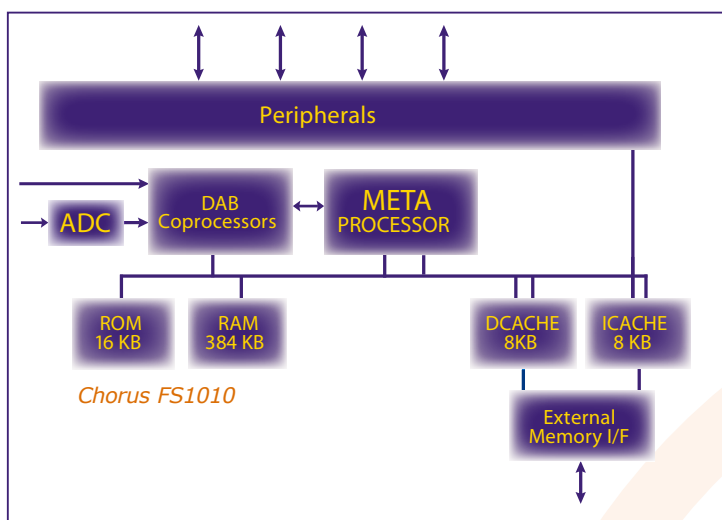
Chorus 1 FS1010

Advanced Programmable Multimedia Processor



OVERVIEW

The Frontier Silicon Chorus FS1010 processor is a super-integrated low-power system-on-chip (SoC) which delivers a highly flexible and efficient solution for multimedia and communication applications such as digital radios, portable music players, and home/in-car audio and multimedia. Chorus uses the revolutionary multi-threaded META™ DSP and general purpose processor core from Imagination Technologies. It integrates on-chip RAM and caches, DAB coprocessors, and a comprehensive range of peripherals. In addition it has extensive applications software and development support.



The multi-threaded architecture of the META core allows Chorus to execute multiple real-time multimedia and communication-based DSP tasks, as well as general-purpose activities such as the user interfacing and data storage/filing needed in multimedia applications. On-chip coprocessors coupled with real-time-aware hardware thread-scheduling enable Chorus to run multiple applications including the concurrent processing of digital radio and other multimedia tasks. For example, a Chorus running at 150 MHz needs only about 25% of its processing capacity to execute the demodulation, decoding, protocol stack and user interface tasks for a digital radio.

The processing power and programmability of Chorus enable it to be used for demanding application-specific functions such as surround sound decoding, audio encoding or advanced data service decoding. Chorus also supports secure operation, using RSA to transfer cryptographic keys or other encrypted data held in external memory to internal memory whilst ensuring that the data can only be read by the intended application code.

Chorus uses dynamic and static power management techniques including fully-static design, clock-gating and inactive period state minimisation for low power usage without compromising performance. The processor clock is generated by a PLL which can be reprogrammed dynamically, enabling power consumption to be minimized for each application.

APPLICATIONS

- Portable digital radios
- Portable music players
- Car radio and audio systems
- Home audio and multimedia systems
- Multimedia-enhanced PDAs
- Advanced digital radios (On-demand and data services)
- Digital music servers/jukeboxes

digital radio

FEATURES

SUPER-INTEGRATION

- META core with four threads and powerful DSP and general-purpose capabilities
- Integrated 384 KB on-chip RAM
- Coprocessors for Digital Radio
- Data & code cache and MMU
- Extensive peripherals
- On-chip ADC
- Secure on-chip RAM area

SINGLE CHIP DAB DIGITAL RADIO BASEBAND CAPABILITY

- For a complete DAB implementation only need external front-end RF, audio D-to-A, Boot FLASH and keypad/display
- On-chip cache optimises performance when larger code space requires external SDRAM
- Decodes full DAB multiplex
- Conforms to ETS 300 401 for all DAB modes and RF bands
- Supports PAD and packet data decoding
- Supports enhanced data services such as EDLS, EPG and CA

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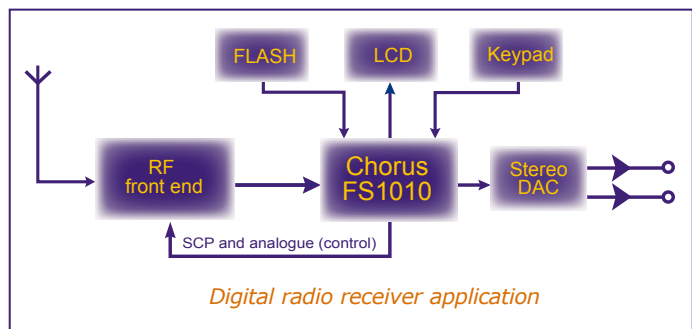
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- Complete software package - DAB decoder object code and reference MMI source code
- Ideal for DAB on-demand and data services
- Processor can run other applications simultaneously with DAB, e.g. MP3, AAC, UI, filing system, content security, etc.



EXTENSIVE ON-CHIP PERIPHERALS

- 16-bit memory port, supporting SDRAM, SRAM, FLASH and I/O expansion
- SPI port supporting 3 devices such as SD card and serial FLASH memories
- LCD port, compatible with graphic and alphanumeric displays
- GPIO for keypad input and general control functions
- USB 1.1 slave port
- 2 buffered asynchronous serial ports
- Digital audio input and output in serial I²S and S/PDIF formats
- RDI output
- 2 ports for control of Serial Control Bus RF front-end and general interfacing
- 4 PDM low-speed DACs for control of RF front-end, power management, display brightness, etc.
- 8-bit bidirectional host port
- JTAG port supports debug and test, giving access to all on-chip features

PROGRAMMABLE AND FLEXIBLE

- Programmable META core with both DSP and RISC instructions is suitable for many multimedia applications
- Easy-to-use multi-threading and automatic hardware scheduler for straightforward integration of real-time applications

ULTRA-LOW POWER

- Designed for low power consumption - less than 100 mW for DAB Digital Radio stereo audio decode, including MMI

HIGH PERFORMANCE

- Very high performance DSP
 - Four 16 x 16 multiply/accumulate operations in one cycle
 - Two 24 x 24 multiply/accumulate operations in one cycle
 - 16-bit radix-2 FFT butterfly operation in one cycle
 - Digital Radio decoding at 30 MIPs
 - MP3 decoding at 9 MIPs
 - AAC stereo sound decoding at 15 MIPs
 - AC3 stereo sound decoding at 20 MIPs
- High performance general-purpose capability
 - Up to 150 MHz 32-bit RISC capability

TOOL AND SOFTWARE SUPPORT

- Comprehensive toolkit support including compiler, assembler and debugger
- A range of evaluation and development systems
- MEOS[®] pre-emptive real-time kernel supports a range of facilities, including device drivers for Chorus peripherals and SD-card file system
- Nucleus support

SMALL 179-PIN BGA PACKAGE

actual size

Supply voltage	Core: 1.8 V \pm 10% I/O: 3.3 V \pm 10%
PLL reference clock	24.576 MHz
Core clock	0 to 150 MHz
Package	179 pin BGA
Operating temperature	-40 to +85°C
Process technology	0.18 μ m CMOS

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